CLAIMS

We claim:

1. An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of approximately same impedance elemental impedance devices, said string having first and second end terminals;

a plurality of wiper switches each coupled between the wiper terminal and the first string; and

a bulk impedance device having a first end coupled to the first end terminal of the first string, an opposite second end, and an impedance value greater than an impedance of the string of elemental impedance devices,

wherein the string and the bulk impedance device are between the first and second reference terminals, and the second end terminal of the first string and the second end of the bulk impedance device are each switchable between a coupling to the first reference terminal and a coupling to the second reference terminal.

2. The digital potentiometer of claim 1, further comprising first and second switching devices operable to implement the switchable coupling of the first end terminal of the first string to the first and second reference terminals, and the switchable coupling of the second end of the bulk impedance device to the first and the second reference terminal, in a complementary manner,

wherein the first switching device is coupled between the first end terminal of the first string, the first reference terminal, and the second reference terminal, and the second switching device is coupled between the second end of the bulk impedance device, the first reference terminal, and the second reference terminal.

3. The digital potentiometer of claim 2, wherein first switching device includes a first transistor coupled between the first end terminal of the first string and the first reference terminal, and a second transistor coupled between the first end terminal of the first string and the second reference terminal, and

wherein the second switching device includes a first transistor coupled between the second end of the bulk impedance device and the second reference terminal, and a second transistor coupled between the second end of the bulk impedance device and the first reference terminal.

4. The digital potentiometer of claim 2, wherein the first and second switching devices are controlled based on a most significant bit of an input n-bit wiper address.

5. The digital potentiometer of claim 1, wherein the switchable coupling of the first end terminal of the first string and the second end of the bulk impedance device are controlled in a complementary manner based on a most significant bit of an input n-bit wiper address.

6. The digital potentiometer of claim 5, wherein a switching of the wiper switches is controlled based on bits of the input n-bit wiper address other than the most significant bit of the wiper address.

7. The digital potentiometer of claim 1, wherein the impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

8. The digital potentiometer of claim 7 wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, and 2^{n-1} said wiper switches.

9. The digital potentiometer of claim 1, wherein the impedance of the first string is less than the impedance of the bulk impedance device by an amount approximately equal to the impedance of one of the elemental impedance devices.

10. The digital potentiometer of claim 1 wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, 2^{n-1} said wiper switches, the impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices, and the complementary switching of the first end terminal of the first string and the second end of the bulk impedance device is controlled based on a most significant bit of an input n-bit wiper address.

11. An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of 2^{n-1}-1 approximately same impedance elemental impedance devices, wherein a first end of the string is coupled to the wiper terminal;

a plurality of wiper switches each coupled between the wiper terminal and the string; and

at least one bulk impedance device, wherein the at least one bulk impedance device has an impedance approximately 2^{n-1} times the impedance of one of the elemental impedance devices, and the string and the at least one bulk impedance device are disposed between the first and second reference terminals.

12. The digital potentiometer of claim 11, further comprising at least one switching device, wherein operation of the at least one switching device causes the string to alternate between providing wiper positions in a lower half of the 2^n wiper positions and in an upper half of the 2^n wiper positions.

13. The digital potentiometer of claim 12, wherein the at least one bulk impedance device is a single bulk impedance device, and the single bulk impedance device is coupled to the first end of the string.

14. The digital potentiometer of claim 12 wherein the string has a second end opposite the first end, the at least one switching device is two switching devices, with one of the two switching devices coupled between the second end of the string and the first reference terminal, and the other of the two switching devices coupled between the single bulk impedance device and the second reference terminal.

15. The digital potentiometer of claim 12, wherein the string alternates between providing wiper positions in a lower half of the 2^n wiper positions and in an upper half of the 2^n wiper positions during operation of the digital potentiometer.

16. The digital potentiometer of claim 11, wherein the at least one bulk impedance device is first and second bulk impedance devices, the at least one switching device is first and second switching devices, and the string includes a second end opposite the first end, and

wherein the first bulk impedance device and the first switching device are coupled to the first end of the string and the first reference terminal, with the first switching device being operable to bypass the first bulk impedance device, and the second bulk impedance device and the second switching device are coupled to the second end of the string and the second reference terminal, with the second switching device being operable to bypass the second bulk impedance device.

17. The digital potentiometer of claim 16, wherein the first and second switching devices are operable in a complementary manner based on a most significant bit of an input n-bit wiper address.

18. The digital potentiometer of claim 12, wherein the at least one bulk impedance device is first and second bulk impedance devices, the at least one switching device is first and second switching devices, the first switching device is operable to bypass the first bulk impedance device, and the second switching device is operable to bypass the second bulk impedance device.

19. The digital potentiometer of claim 18, wherein the first and second switching devices are operable in a complementary manner based on a most significant bit of an input n-bit wiper address.

20. An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of approximately same impedance elemental impedance devices;

at least one bulk impedance device, wherein the string and the at least one bulk impedance device are disposed between the first and second reference terminals, and the at least one bulk impedance device has an impedance greater than an impedance of the string;

a plurality of wiper switches each coupled between the wiper terminal and the string; and

a control circuit that receives an input n-bit wiper address, and based thereon controls both a switching of the wiper switches and a selection between having the string provide wiper positions in a lower half of the 2^n wiper positions and in an upper half of the 2^n wiper positions.

21. The digital potentiometer of claim 20, wherein the control circuit selects between having the string provide

wiper positions in the lower half of the 2^n wiper positions and in the upper half of the 2^n wiper positions based on a first subportion of the input n-bit wiper address, and controls the switching of the wiper switches based on a different second subportion of the n-bit wiper address.

22. The digital potentiometer of claim 20, wherein the at least one bulk impedance device is a single bulk impedance device.

23. The digital potentiometer of claim 19, wherein the at least one bulk impedance device is a first bulk impedance device and a second bulk impedance device, with the first bulk impedance device being coupled between a first end of the string and the first reference terminal, and the second bulk impedance device being coupled between an opposite second end of the string and the second reference terminal, and

wherein the control circuit controls a selective bypassing of the first bulk impedance device, and a selective bypassing of the second bulk impedance device.

24. A method of operating an n-bit digital potentiometer having 2^n impedance units between a first reference terminal and a second reference terminal, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of elemental impedance and a bulk impedance device between the first and second reference terminals, the bulk impedance device having an impedance greater than an impedance of the first string, wherein a first end of the string is coupled to a first end of the bulk impedance device;

alternating a coupling of the second end of the first string and the second end of the bulk impedance device to the first reference terminal and to the second reference terminal based on the first n-bit wiper address; and

tapping the first string based on the first n-bit wiper address.

25. The method of claim 24, wherein the step of alternating the coupling is based on only a most significant bit of the n-bit wiper address.

26. The method of claim 24, wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, and an impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

27. A method of operating an n-bit digital potentiometer having 2^n wiper positions, a first reference terminal and a second reference terminal, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of 2^{n-1}-1 approximately same impedance elemental impedance devices and at least one bulk impedance between the first and second reference terminals, the at least one bulk impedance device having an impedance approximately 2^{n-1} times the impedance of one of the elemental impedance devices;

alternating the first string between providing impedance in a lower half of the 2^n wiper positions and an upper half of the 2^n wiper positions based on a first subportion of the n-bit wiper address, with the at least one bulk impedance device providing impedance in the one of the lower half and the upper half of the 2^n wiper positions not provided by the first string; and

tapping the first string based on a second subportion of the n-bit wiper address.

28. The method of claim 27, wherein the at least one bulk impedance device is a single bulk impedance device, and the step of alternating the first string comprises:

coupling the first string to the first reference terminal to have the first string provide impedance in the lower half of the 2^n wiper positions and to the second reference terminal to provide impedance in the upper half of the 2^n wiper positions, and coupling the single bulk impedance device to the one of the first and second reference terminals not coupled to the first string.

29. The method of claim 28, wherein a first structure also is between the first and second reference terminals, said first structure comprising an impedance device and a permanently-on switch.

30. The method of claim 27, wherein the at least one bulk impedance device comprises two bulk impedance devices, with one of the bulk impedance devices being coupled between the first reference terminal and a first end of the first string and the other of the bulk impedance devices being coupled between the second reference terminal and a second end of the first string, and

wherein the step of alternating the first string comprises bypassing one of the bulk impedance devices and not bypassing the other of the bulk impedance devices.

31. The method of claim 30, wherein a first structure also is between the first and second reference terminals, said first structure comprising an impedance device and a permanently-on switch.

32. The method of claim 27, wherein a first structure also is between the first and second reference terminals, said first structure comprising an impedance device and a permanently-on switch.

33. An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and an wiper terminal;

a first string of approximately same impedance elemental impedance devices, said first string having opposed first and second end terminals;

a plurality of wiper switches each coupled between the wiper terminal and the first string; and

at least one bulk impedance device having an impedance greater than an impedance of the first string,

wherein the first string and the at least one bulk impedance device are disposed between the first and second reference terminals, and

wherein the at least one bulk impedance device is coupled between the first reference terminal and the first string when an input n-bit wiper address has a logical one most significant bit and is coupled between the second reference terminal and the first string when the most significant bit of the input n-bit wiper address is a logical zero.

34. The digital potentiometer of claim 33, wherein the at least one bulk impedance device is a single bulk impedance device selectively coupleable to the first and second reference terminals.

35. The digital potentiometer of claim 33, wherein the at least one bulk impedance device comprises first and second bulk impedance devices, with the first bulk impedance device being coupled between the first reference terminal and the first end terminal of the first string, and the second bulk impedance device being coupled between the second reference terminal and the second end terminal of the first string, and

wherein a first switching device is coupled to the first reference terminal, and second switching device is coupled to the second reference terminal, the first switching device being operable to bypass the first bulk impedance device, and the second switching device being operable to bypass the second bulk impedance device.

36. The digital potentiometer of claim 33, further comprising mirror image second and third strings of shunted impedance devices also between the first and second reference terminals, wherein an impedance of each of the second and third strings is between the impedance of the first string and the impedance of the at least one bulk resistor.

37. An n-bit digital potentiometer including 2^n wiper addresses, comprising:

a first reference terminal, an opposite second reference terminal, and an wiper terminal;

a first string of approximately same impedance elemental impedance devices, said string having opposed first and second end terminals;

a plurality of wiper switches each coupled between the wiper terminal and the first string;

first and second bulk impedance devices each of an approximately same impedance greater than an impedance of the first string, wherein the first string, the first bulk impedance device, and the second bulk impedance devices are between the first and second reference terminals;

a first switching device operable for selectively bypassing the first bulk impedance device; and

a second switching device operable for selectively bypassing the second bulk impedance device.

38. The digital potentiometer of claim 37, wherein switching of the first and second switching devices is controlled based on a most significant bit of an input n-bit wiper address.

39. The digital potentiometer of claim 38, wherein switching of the respective wiper switches is controlled based on bits of the n-bit wiper address lesser than the most significant bit, and not based on the most significant bit.

40. The digital potentiometer of claim 37, wherein the impedance of each of the first and second bulk impedance devices is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

41. The digital potentiometer of claim 40 wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, and 2^{n-1} said wiper switches.

42. The digital potentiometer of claim 37, wherein the impedance of the first string is less than the impedance of each of the first and second bulk impedance devices by an amount approximately equal to the impedance of one of the elemental impedance devices.

43. The digital potentiometer of claim 37, wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, 2^{n-1} said wiper switches, the impedance of each of the first and second bulk impedance devices is approximately 2^{n-1} times the impedance of one of the elemental impedance devices, and switching of the first and second switching devices is controlled based on a most significant bit of an input n-bit wiper address.

44. The digital potentiometer of claim 37, further comprising a control circuit coupled to the first and second switching devices, said control circuit operable for switching the first switching device complementary to switching the second switching device, whereby one of the first and second bulk impedance devices is bypassed and the other is not bypassed.

45. The digital potentiometer of claim 37, wherein the first bulk impedance device is coupled to the first end terminal of the first string and the first reference terminal, and the second bulk impedance device is coupled to the second end terminal of the first string and the second reference terminal.

46. The digital potentiometer of claim 45, wherein switching of the first and second switching devices is controlled based on a most significant bit of an input n-bit wiper address, and switching of the respective wiper switches is controlled based on bits of the n-bit wiper address lesser than the most significant bit, and not based on the most significant bit.

47. The digital potentiometer of claim 45, further comprising:

mirror image second and third strings of approximately same impedance intermediate impedance devices, with the impedance of each of the second and third strings being between the impedance of the first string and the impedance of one of the bulk impedance devices,

wherein the first, second, and third strings and the first and second bulk impedance devices are between the first and second reference terminals.

48. The digital potentiometer of claim 47, further comprising:

a first set of shunt switches each coupled between a first common node and a respective one of a plurality of nodes of the second string, with one of said plurality of nodes being between each adjacent pair of the intermediate impedance devices and one said node being at an end of the last intermediate impedance device of the second string, wherein the respective shunt switches are operable to bypass any impedance device of the second string between the respective node and the first common node; and

a second set of shunt switches in a mirror image configuration to the first set of shunt switches, each said shunt switch coupled between a second common node and a respective one of a plurality of nodes of the third string, with one of said plurality of nodes being between each adjacent pair of the intermediate impedance devices and one said node being at an end of the last intermediate impedance device of the third string, wherein the respective shunt switches are operable to bypass any impedance device of the third string between the respective node and the second common node.

49. The digital potentiometer of claim 48, wherein the digital potentiometer includes $2^{[n/2]}$-1 said elemental impedance devices in the first string, $2^{[n/2]}$ wiper switches, $2^{[(n-1)/2]}$-1 said intermediate impedance devices in each of the second and third strings, with the impedance of each of said intermediate impedance device being approximately $2^{[n/2]}$ times one of said elemental impedance devices, $2^{[(n-1)/2]}$-1 said shunt switches in each of the first and second sets of shunt switches, and the impedance of each of said first and second bulk impedance devices is approximately 2^{n-1} times one of the elemental impedance devices.

50. The digital potentiometer of claim 48, further comprising a control circuit coupled to the first and second switching devices, said control circuit operable for switching the first switching device complementary to switching the second switching device, and for switching the shunt switches of the first and second sets of shunt switches in a manner that maintains a constant impedance between the first and second reference terminals due to the second and third strings.

51. The digital potentiometer of claim 48, further comprising a control circuit coupled to the first and second switching devices, said control circuit operable for switching the first switching device complementary to switching the second switching and for switching the shunt switches of the first set in an inverse complementary manner to the switching of the shunt switches of the second set.

52. The digital potentiometer of claim 48, wherein the first bulk impedance device is coupled to the first common node, and the second bulk impedance device is coupled to the second common node.

53. The digital potentiometer of claim 48, wherein the first bulk impedance device is between the first reference terminal and the second string, and the second bulk impedance device is between the second reference terminal and the third string.

54. The digital potentiometer of claim 48, wherein the first bulk impedance device is between the first and second strings, and the second bulk impedance device is between the first and third strings.

55. The digital potentiometer of claim 37, further comprising:

mirror image second and third strings of approximately same impedance intermediate impedance devices, with an impedance of each of the second and third strings being between the impedance of the first string and the impedance of one of the bulk impedance devices, wherein the first, second, and third strings and the first and second bulk impedance devices are between the first and second reference terminals;

a first set of shunt switches each coupled between a first common node and a respective one of a plurality of nodes of the second string; and

a second set of shunt switches in a mirror image configuration to the first set of shunt switches, each said shunt switch coupled between a second common node and a respective one of a plurality of nodes of the third string.

56. The digital potentiometer of claim 55, further comprising a control circuit coupled to control switching of the first and second switching devices, switching of the wiper switches, and switching of the shunt switches of the first and second set of shunt switches.

57. The digital potentiometer of claim 56, wherein the control circuit is operable for switching the first and second switching devices in a complementary manner, and for switching the shunt switches of the first set in an inverse complementary manner relative to the shunt switches of the second set.

58. The digital potentiometer of claim 55, further comprising a plurality of first structures between the first and second reference terminals, each said first structure comprising an impedance device in parallel with a permanently-on switch.

59. The digital potentiometer of claim 58, wherein a first one of the first structures is coupled between a first impedance device of the second string and the first common node, and a second one of the first structures is coupled between a first impedance device of the third string and the second common node.

60. The digital potentiometer of claim 59, wherein a third one of the first structures is coupled to the first bulk impedance device, and the first switching device is operable for bypassing both the first bulk impedance device and the third first structure, and a fourth one of the first structures is coupled to the second bulk impedance device, and the second switching device is operable for bypassing both the second bulk impedance device and the fourth first structure.

61. The digital potentiometer of claim 60, wherein the first bulk impedance device is between the first and the second strings, and the second bulk impedance device is between the first and the third strings.

62. The digital potentiometer of claim 60, wherein the first bulk impedance device is between the first reference terminal and the second string, and the second bulk impedance device is between the second reference terminal and the third string.

63. The digital potentiometer of claim 59, wherein a first one of the first structures is coupled to the first bulk impedance device, and the first switching device is operable for bypassing both the first bulk impedance device and the first of the first structure, and a second one of the first structures is coupled to the second bulk impedance device, and the second switching device is operable for bypassing both the second bulk impedance device and the second one of the first structures.

64. The digital potentiometer of claim 63, wherein the first bulk impedance device is between the first and the second strings, and the second bulk impedance device is between the first and the third strings.

65. The digital potentiometer of claim 63, wherein the first bulk impedance device is between the first reference terminal and the second string, and the second bulk impedance device is between the second reference terminal and the third string.

66. The digital potentiometer of claim 55, wherein the digital potentiometer includes $2^{[n/2]}$-1 said elemental impedance devices in the first string, $2^{[n/2]}$ wiper switches, $2^{[(n-1)/2]}$-1 said intermediate impedance devices in each of the second and third strings, with the impedance of each of said intermediate impedance device being approximately $2^{[n/2]}$ times one of said elemental impedance devices, $2^{[(n-1)/2]}$-1 said shunt switches in each of the first and second sets of shunt switches, and the impedance of each of said first and second bulk impedance devices is approximately 2^{n-1} times one of the elemental impedance devices.

67. The digital potentiometer of claim 55, further comprising a control circuit coupled to control switching of the first and second switching devices, switching of the wiper switches, and switching of the shunt switches of the first and second sets of shunt switches,

wherein the control circuit is operable for switching the first and second switching devices in a complementary manner, and for switching the shunt switches of the first set in an inverse complementary manner relative to the shunt switches of the second set.

68. The digital potentiometer of claim 55, wherein switching of the first and second switching devices is based on a most significant bit of an n-bit input wiper address, switching of the first and second sets of shunt switches is based on a second subset of the bits of the n-bit wiper address lesser than most significant bit, and switching of the wiper switches is based is a third subset set of the bits of the n-bit wiper address lesser than the second set of bits.

69. An n-bit digital potentiometer including 2^n wiper addresses, comprising:

a first reference terminal, an opposite second reference terminal, and an wiper terminal;

a first string of approximately same impedance elemental impedance devices;

a plurality of wiper switches each coupled between the first string and the wiper terminal;

mirror image first and second bulk impedance devices of an approximately same impedance greater than an impedance of the first string; and

mirror image second and third strings of approximately same impedance intermediate impedance devices, with the impedance of each of the second and third strings being between the impedance of the first string and the impedance of one of the bulk impedance devices,

wherein the first, second, and third strings and the first and second bulk impedance devices are between the first and second reference terminals, with the first bulk impedance device and the second string being between the first reference terminal and the first string, and the second bulk impedance device and the third string being between the first string and the second reference terminal.

70. The digital potentiometer of claim 69, wherein the digital potentiometer includes $2^{[n/2]}$-1 said elemental impedance devices in the first string, $2^{[n/2]}$ wiper switches, $2^{[(n-1)/2]}$-1 said intermediate impedance devices in each of the second and third strings, with the impedance of each said intermediate impedance device being approximately $2^{[n/2]}$ times one of said elemental impedance devices, and the impedance of each of said first and second bulk impedance devices is approximately 2^{n-1} times one of the elemental impedance devices.

71. The digital potentiometer of claim 69, wherein the first and second bulk impedance devices are each selectively bypassable, the entire second and third strings are each selectively bypassable, and at least one subset of each the second and third strings is selectively bypassable.

72. The digital potentiometer of claim 75, wherein the selective bypassing of the first and second bulk impedance devices is based on a most significant bit of an n-bit input wiper address, the selective bypassing of the entire second and third strings and the bypassing of the at least one subset of the first and second strings is based on a second subset of the bits of the n-bit wiper address lesser than most significant bit, and switching of the wiper switches is based is a third subset set of the bits of the n-bit wiper address lesser than the second set of bits.

73. The digital potentiometer of claim 72, wherein the first bulk impedance device is between first and second strings, and the second bulk impedance device is between the first and third strings.

74. The digital potentiometer of claim 72, wherein the first bulk impedance device is between first reference terminal and the second string, and the second bulk impedance device is between the second reference terminal and the third string.

75. The digital potentiometer of claim 69, further comprising:

a first switching device operable for selectively bypassing the first bulk impedance device;

a second switching device operable for selectively bypassing the second bulk impedance device;

a first set of shunt switches each coupled between a first common node and a respective one of a plurality of nodes of the second string; and

a second set of shunt switches in a mirror image configuration to the first set of shunt switches, with each said shunt switch coupled between a second common node and a respective one of a plurality of nodes of the third string.

76. The digital potentiometer of claim 75, further comprising a control circuit operable for switching the wiper switches, switching the first and second switching devices in a complementary manner, and switching the shunt switches of the first set in an inverse complementary manner relative to the shunt switches of the second set.

77. The digital potentiometer of claim 69, further comprising a plurality of first structures also between the first and second reference terminals, each said first structure comprising an impedance device in parallel with a permanently-on switch.

78. A digital potentiometer comprising:

a first reference terminal, and second reference terminal, and a plurality of impedance devices between the first and second reference terminals; and

at least one first structure, with each said first structure comprising a permanently-on switch in parallel with one of the impedance devices.

79. The digital potentiometer of claim 78, wherein each said first structure is bypassable by at least one switching device.

80. The digital potentiometer of claim 78, wherein there are a plurality of said first structures and a plurality of the switching devices, with each switching device being operable to bypass at least one of the first structures.

81. The digital potentiometer of claim 80, wherein each said switching device is also operable to bypass at least one other said impedance device.

82. The digital potentiometer of claim 80, wherein at least some of said first structures are bypassable by a plurality of the switching devices.

83. The digital potentiometer of claim 78, wherein the plurality of impedance devices comprises:

a first string of approximately same impedance elemental impedance devices;

mirror image bypassable first and second bulk impedance devices of an approximately same impedance greater than an impedance of the first string; and

mirror image bypassable second and third strings of approximately same impedance intermediate impedance devices, with the impedance of each of the second and third strings being between an impedance of the first string and the impedance of one of the bulk impedance devices.

84. The digital potentiometer of claim 83, wherein there are a plurality of first structures, with a respective one of the first structures being coupled to a first intermediate impedance device of the second and third strings.

85. The digital potentiometer of claim 83, wherein there are a plurality of first structures, with a first one of the first structures being coupled to the first bulk impedance device, and a second one of said first structures being coupled to the second bulk impedance device.

86. A digital potentiometer including 2^n wiper positions, comprising:

a first string of approximately same resistance elemental resistors coupled in series;

mirror image first and second bulk resistors of an approximately same resistance greater than a resistance of the first string; and

mirror image second and third strings of approximately same resistance intermediate resistors in series, with a resistance of each of the second and third strings being between the resistance of the first string and the resistance one of the bulk resistors; and

a plurality of first structures, each said first structure comprising an resistor in parallel with a permanently-on switch,

wherein the first, second, and third strings, the first and second bulk resistors, and the plurality of first structures are in series between the first and second reference terminals, with the first bulk resistor, the second string, and at least one of the first structures being between the first reference terminal and the first string, and the second bulk resistor, the third string, and at least one of the first structures being between the first string and the second reference terminal, and

wherein the first and second bulk resistors are each selectively bypassable, the entire second and third strings are each selectively bypassable, and at least one subset of each of the second and third strings is selectively bypassable.

87. A method of operating an n-bit digital potentiometer including 2^n wiper positions, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of elemental impedance devices and first and second bulk impedance devices between first and second reference terminals, the first and second bulk impedance devices having an approximately same impedance greater than an impedance of the first string; and

determining based on the n-bit wiper address which one of the first and second bulk impedance devices to have bypassed and which one not to have bypassed.

88. The method of claim 87, wherein the step of determining is based on a most significant bit of the n-bit wiper address.

89. The method of claim 87, wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, and an impedance of the first and second bulk impedance devices is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

90. The method of claim 88, further comprising:

bypassing one of the first bulk impedance device and the second bulk impedance device and not bypassing the other of the first bulk impedance device and the second bulk impedance device; and

tapping the first string.

91. The method of claim 87, further comprising:

bypassing one of the first bulk impedance device and the second bulk impedance device and not bypassing the other of the first bulk impedance device and the second bulk impedance device; and

tapping the first string.

92. The method of claim 91, wherein the bypassing of one of the first and second bulk impedance devices is based on a first subset of the n-bit wiper address, and the tapping of the first string based on a second subset of the n-bit wiper address lesser than the first subset.

93. The method of claim 87, wherein the digital potentiometer includes mirror image second and third strings of approximately same impedance intermediate impedance devices also between the first and second reference terminals, with an impedance of each of the second and third strings being between an impedance of the first string and the impedance of one of the bulk impedance devices, and further comprising:

determining based on the n-bit wiper address whether to have a set of the intermediate impedance devices of the second string bypassed and whether to have a set of the intermediate impedance devices of the third string bypassed.

94. The method of claim 93, further comprising:

bypassing a set of the intermediate impedance devices of the second string and not bypassing a set of the intermediate impedance devices of the third string; and

tapping the first string.

95. The method of claim 93 further comprising:

bypassing none of the intermediate impedance devices of the one of the second and third strings and bypassing all of the intermediate impedance devices of the other of the second and third strings; and

tapping the first string.

96. The method of claim 93, further comprising:

bypassing one of the first bulk impedance device and the second bulk impedance device and not bypassing the other of the first bulk impedance device and the second bulk impedance device; and

tapping the first string.

97. The method of claim 96, further comprising:

bypassing a set of the intermediate impedance devices of the second string and not bypassing an inverse corresponding set of the intermediate impedance devices of the third string; and

tapping the first string.

98. The method of claim 96, further comprising:

bypassing none of the intermediate impedance devices of the one of the second and third strings and bypassing all of the intermediate impedance devices of the other of the second and third strings; and

tapping the first string.

99. The method of claim 93, wherein the digital potentiometer includes $2^{[n/2]}$-1 said elemental impedance devices in the first string, $2^{[(n-1)/2]}$-1 said intermediate impedance devices in each of the second and third strings, with the impedance of each said intermediate impedance device being approximately $2^{[n/2]}$ times one of said elemental impedance devices, and the impedance of each of said first and second bulk impedance devices is approximately 2^{n-1} times one of the elemental impedance devices.

100. The method of claim 93, wherein the step of determining which one of the first and second bulk impedance devices to have bypassed and which one not to have bypassed is based on a first subportion of the n-bit wiper address, the step of determining whether to have a set of the intermediate impedance devices of the second string bypassed and whether to have a set of the intermediate impedance devices of the third string bypassed is based on a lesser second subportion of the n-bit wiper address, and tapping the first string is based on a still-lesser third subportion of the n-bit wiper address.

101. The method of claim 93, further comprising:

bypassing some of the intermediate impedance devices of the second string and not bypassing a remainder of the intermediate impedance devices of the second string,

bypassing some of the intermediate impedance devices of the third string and not bypassing a remainder of the intermediate impedance devices of the second string,

wherein a count of the intermediate impedance devices of the first string bypassed equals a count of the intermediate impedance devices of the second string not bypassed, and a count of the intermediate impedance devices of the first string not bypassed equals a count of the intermediate impedance devices of the third string bypassed.

102. The method of claim 93, wherein the digital potentiometer includes mirror image second and third strings of approximately same impedance intermediate impedance devices also between the first and second reference terminals, with an impedance of each of the second and third strings being between an impedance of the first string and the impedance of one of the bulk impedance devices, and the second and third strings having a corresponding first intermediate

impedance device and a corresponding last intermediate impedance device, and further comprising:

bypassing a contiguous first subset of the intermediate impedance devices of the second string including the first intermediate impedance device and not bypassing a contiguous second subset of the impedance devices of the second string including the last intermediate impedance device, the second subset including any impedance device of the second string outside of the first subset; and

not bypassing a contiguous first subset of the intermediate impedance devices of the third string including the last intermediate impedance device and bypassing a contiguous second subset of the intermediate impedance devices of the second string including the first intermediate impedance device, the second subset including any impedance device of the string outside of the first subset,

wherein the first subset of the second string includes a same number of the intermediate impedance devices as the first subset of the third string, and the second subset of the second string includes a same number of the intermediate impedance devices as the second subset of the third string.

103. The method of claim 87, wherein the digital potentiometer further includes a plurality of first structures also between the first and second reference terminals, each said first structure including an impedance device in parallel with a permanently-on switch.

104. The method of claim 103, further comprising:

bypassing half of the first structures, and not bypassing a remaining half of the first structures.

105. A method of operating an n-bit digital potentiometer including 2^n wiper positions, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of elemental impedance devices and first and second bulk impedance devices between first and second reference terminals, the first and second bulk impedance devices having an approximately same impedance greater than an impedance of the first string;

bypassing one of the first bulk impedance device and the second bulk impedance device and not bypassing the other of the first bulk impedance device and the second bulk impedance device; and

tapping the first string.

106. The method of claim 105, wherein the steps of bypassing and not bypassing are based on a most significant bit of the n-bit wiper address.

107. The method of claim 106, wherein the step of tapping is based on a subset of the n-bit wiper address not including the most significant bit.

108. The method of claim 105, wherein the digital potentiometer further includes:

mirror image second and third strings of approximately same impedance intermediate impedance devices also between the first and second reference terminals, with an impedance of each of the second and third strings being between an impedance of the first string and the one of the bulk impedance devices, the first bulk impedance device and the second string being between the first reference terminal and the first string, and the second bulk impedance device and the third string being between the first string and the second reference terminal.

109. The method of claim 108, further comprising:

bypassing a set of the intermediate impedance devices of the second string and not bypassing an inverse corresponding set of the intermediate impedance devices of the third string.

110. The method of claim 108, further comprising:

bypassing some of the intermediate impedance devices of the second string and not bypassing a remainder of the intermediate impedance devices of the second string; and

bypassing some of the intermediate impedance devices of the third string and not bypassing a remainder of the intermediate impedance devices of the second string.

111. The method of claim 110, wherein a count of the intermediate impedance devices of the first string bypassed equals a count of the intermediate impedance devices of the second

string not bypassed, and a count of the intermediate impedance devices of the first string not bypassed equals a count of the intermediate impedance devices of the third string bypassed.

112. The method of claim 110, wherein bypassing one of the first and second bulk impedance devices is based on a first subset of an n-bit input wiper address, bypassing the some of the intermediate impedance devices is based on a second subset of the bits of the n-bit wiper address lesser than most significant bit, and tapping the first string is based is a third subset set of the bits of the n-bit wiper address lesser than the second set of bits.

113. The method of claim 108, wherein the second and third strings include a corresponding first intermediate impedance device and a corresponding last intermediate impedance device, and further comprising:

bypassing a contiguous first subset of the intermediate impedance devices of the second string including first intermediate impedance device and not bypassing a contiguous second subset of the impedance devices of the second string including the last intermediate impedance device, the second subset including any impedance device of the second string outside of the first subset; and

not bypassing a contiguous first subset of the intermediate impedance devices of the third string including the last intermediate impedance device and bypassing a contiguous second subset of the intermediate impedance devices of the second string including the first intermediate impedance device, the second subset including any impedance device of the string outside of the first subset,

wherein the first subset of the second string includes a same number of the intermediate impedance devices as the first subset of the third string, and the second subset of the first string includes a same number of the intermediate impedance devices as the second subset of the third string.